In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1   1.   (Currently Amended) A multiply-accumulate module comprising:

2   a multiply-accumulate core, wherein said multiply-accumulate

3   core comprises:

4   a plurality of Booth encoder cells;

5   a plurality of Booth decoder cells connected to at least

6   one of said Booth encoder cells, said plurality of Booth decoder

7   cells including at least one first Booth decoder cell and at least

8   one second Booth decoder cell, said at least one first Booth

9   decoder cell structurally the same as said at least one second

10   Booth decoder cells; and

11   a plurality of Wallace tree cells connected to at least

12   one of said Booth decoder cells, said plurality of Wallace tree

13   cells including at least one first Wallace tree cell and at least

14   one second Wallace tree cell, said at least one first Wallace tree

15   cell structurally the same as said at least one second Wallace tree

16   cell;

17   wherein said multiply-accumulate module includes at least one

18   critical path, said at least one critical path being an electrical

19   path for which an amount of time that it takes for an electrical

20   signal to travel from an input of said multiply-accumulate core to

21   an output of said multiply-accumulate core is greater than or equal

22   to a predetermined amount of time and less than a longest amount of

23   time that it takes any other electrical signal to travel from said

24   input of said multiply-accumulate core to said output of said

25   multiply-accumulate core, wherein said predetermined amount of time

26   is less than said longest amount of time;

27   wherein said at least one first Wallace tree cell or said at

28   least one first Booth decoder cell are disposed on said at least

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29 one critical path;
30   wherein said at least one second Wallace tree cell and said at
31 least one second Booth decoder cell are not disposed on any of said
32 at least one critical path;
33   wherein said at least one first Wallace tree cell or said at
34 least one first Booth decoder cell comprises a first plurality of
35 transistors, and at least one second Wallace tree cell or at least
36 one second Booth decoder cell comprises a second plurality of
37 transistors; and
38   a width of at least one of said first plurality of transistors
39 of said at least one first Wallace tree cell or said at least one
40 first Booth decoder cell is greater than a width of a corresponding
41 one of said second plurality of transistors of a corresponding one
42 of said at least one second Wallace tree cell and said at least one
43 second Booth decoder cell.

2.   (Canceled)

1 3.   (Previously Presented) The multiply-accumulate module of claim
2 1, wherein said multiply-accumulate core further comprises:
3   an adder connected to at least one of said Wallace tree cells;
4   a saturation detector connected to said adder, wherein said
5 multiply-accumulate module further comprises:
6   at least one input register connected to at least one of said
7 Booth encoding cells; and
8   at least one result register connected to said saturation
9 detector.

4 to 8.   (Canceled)

1 9.   (Original) The multiply-accumulate module of claim 1, wherein
2 said at least one second cell is a most significant bit or a least

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3 significant bit and said at least one first cell is not a most
4 significant bit or a least significant bit.

1 10. (Currently Amended) A parallel multiplier comprising:
2   a parallel multiplier core, wherein said parallel multiplier
3 core comprises:
4   a plurality of Booth encoder cells;
5   a plurality of Booth decoder cells connected to at least
6 one of said Booth encoder cells, said plurality of Booth decoder
7 cells including at least one first Booth decoder cell and at least
8 one second Booth decoder cell, said at least one first Booth
9 decoder cell structurally the same as said at least one second
10 Booth decoder cells; and
11   a plurality of Wallace tree cells connected to at least
12 one of said Booth decoder cells, said plurality of Wallace tree
13 cells including at least one first Wallace tree cell and at least
14 one second Wallace tree cell, said at least one first Wallace tree
15 cell structurally the same as said at least one second Wallace tree
16 cell;
17   wherein said multiply-accumulate module includes at least one
18 critical path, said at least one critical path being an electrical
19 path for which an amount of time that it takes for an electrical
20 signal to travel from an input of said multiply-accumulate core to
21 an output of said multiply-accumulate core is greater than or equal
22 to a predetermined amount of time and less than a longest amount of
23 time that it takes any other electrical signal to travel from said
24 input of said multiply-accumulate core to said output of said
25 multiply-accumulate core, wherein said predetermined amount of time
26 is less than said longest amount of time;
27   wherein said at least one first Wallace tree cell or said at
28 least one first Booth decoder cell are disposed on said at least
29 one critical path;

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30   wherein said at least one second Wallace tree cell and said at
31   least one second Booth decoder cell are not disposed on any of said
32   at least one critical path;
33   wherein said at least one first Wallace tree cell or said at
34   least one first Booth decoder cell comprises a first plurality of
35   transistors, and at least one second Wallace tree cell or at least
36   one second Booth decoder cell comprises a second plurality of
37   transistors; and
38   a width of at least one of said first plurality of transistors
39   of said at least one first Wallace tree cell or said at least one
40   first Booth decoder cell is greater than a width of a corresponding
41   one of said second plurality of transistors of a corresponding one
42   of said at least one second Wallace tree cell and said at least one
43   second Booth decoder cell.

11.   (Canceled)

1   12.   (Previously Presented) The parallel multiplier of claim 10,
2   wherein said parallel multiplier core further comprises:
3   an adder connected to at least one of said Wallace tree cells;
4   a saturation detector connected to said adder, wherein said
5   parallel multiplier further comprises:
6   at least one input register connected to at least one of said
7   Booth encoding cells; and
8   at least one result register connected to said saturation
9   detector and at least one of said Wallace tree cells.

13 to 17.   (Canceled)

1   18.   (Original) The multiply-accumulate module of claim 10, wherein
2   at least one second cell is a most significant bit or a least
3   significant bit and at least one first cell is not a most

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4   significant bit or a least significant bit.

1   19. (Currently Amended) A method of designing a multiply-
2   accumulate module comprising the steps of:
3   providing a multiply-accumulate core, wherein the step of
4   providing a multiply-accumulate core comprises the steps of:
5   providing a plurality of Booth encoder cells;
6   connecting a plurality of Booth decoder cells to at least
7   one of said Booth encoder cells;
8   connecting a plurality of Wallace tree cells to at least
9   one of said Booth decoder cells;
10   defining at least one critical path within said
11   multiply-accumulate module, said at least one critical path being
12   an electrical path for which an amount of time that it takes for an
13   electrical signal to travel from an input of said
14   multiply-accumulate core to an output of said multiply-accumulate
15   core is greater than or equal to a predetermined amount of time and
16   less than a longest amount of time that it takes any other
17   electrical signal to travel from said input of said
18   multiply-accumulate core to said output of said multiply-accumulate
19   core, wherein said predetermined amount of time is less than a̶ said
20   longest amount of time;
21   defining a Wallace tree cell disposed on said at least
22   one critical path as a first Wallace tree cell;
23   defining a Wallace tree cell not disposed on any of said
24   at least one critical path as second Wallace tree cell;
25   defining a Booth decoder cell disposed on said at least
26   one critical path as a first Booth decoder cell;
27   defining a Booth decoder cell not disposed on any of said
28   at least one critical path as second Booth decoder cell;
29   constructing each first Wallace tree cell and each first
30   Booth decoder cell of a first plurality of transistors, each first

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31 Wallace tree cell structurally the same as each second Wallace tree
32 cell, and constructing each second Wallace tree cell and each
33 second Booth decoder cell of a second plurality of transistors,
34 each first Booth decoder cell structurally the same as each second
35 Booth decoder cell;
36   selecting a first width for at least one of said first
37 plurality of transistors of at least one of said first Wallace tree
38 cell or said first Booth decoder cell; and
39   selecting a second width for at least one of said second
40 plurality of transistors of a second Wallace tree cell
41 corresponding to said at least one of said first Wallace tree cell
42 or of a second Booth decoder cell corresponding to said first Booth
43 decoder cell which is less than said first width of a corresponding
44 one of said first plurality of transistors.

1   20. (Currently Amended) A method of designing a parallel
2   multiplier comprising the steps of:
3   providing a parallel multiplier core, wherein the step of
4   providing a parallel multiplier core comprises the steps of:
5   providing a plurality of Booth encoder cells;
6   connecting a plurality of Booth decoder cells to at least
7   one of said Booth encoder cells;
8   connecting a plurality of Wallace tree cells to at least
9   one of said Booth decoder cells;
10   defining at least one critical path within said
11 multiply-accumulate module, said at least one critical path being
12 an electrical path for which an amount of time that it takes for an
13 electrical signal to travel from an input of said
14 multiply-accumulate core to an output of said multiply-accumulate
15 core is greater than or equal to a predetermined amount of time and
16 less than a longest amount of time that it takes any other
17 electrical signal to travel from said input of said

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18   multiply-accumulate core to said output of said multiply-accumulate

19   core, wherein said predetermined amount of time is less than a said

20   longest amount of time;

21   defining a Wallace tree cell disposed on said at least

22   one critical path as a first Wallace tree cell;

23   defining a Wallace tree cell not disposed on any of said

24   at least one critical path as second Wallace tree cell;

25   defining a Booth decoder cell disposed on said at least

26   one critical path as a first Booth decoder cell;

27   defining a Booth decoder cell not disposed on any of said

28   at least one critical path as second Booth decoder cell;

29   constructing each first Wallace tree cell and each first

30   Booth decoder cell of a first plurality of transistors, each first

31   Wallace tree cell structurally the same as each second Wallace tree

32   cell, and constructing each second Wallace tree cell and each

33   second Booth decoder cell of a second plurality of transistors,

34   each first Booth decoder cell structurally the same as each second

35   Booth decoder cell;

36   selecting a first width for at least one of said first

37   plurality of transistors of at least one of said first Wallace tree

38   cell or at least one of said first Booth decoder cell; and

39   selecting a second width for at least one of said second

40   plurality of transistors of a second Wallace tree cell

41   corresponding to said at least one of said first Wallace tree cell

42   or of a second Booth decoder cell corresponding to said first Booth

43   decoder cell which is less than said first width of a corresponding

44   one of said first plurality of transistors.

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